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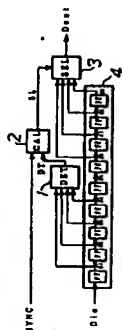
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(54) [発明の名称] フレーム同期装置

(57) [要約]

【目的】 伝送速度の高速化に対応して、配線の間の干渉の侵入を防止するフレーム同期装置を提供することを目的とするものである。

【構成】 伝送路中に送信されてきたフレーム同期パターンの付加されている情報データを伝送する配線手段と、この配線手段に伝送された情報データからこのフレーム同期パターンを抽出するフレーム同期パターン抽出手段と、伝送路中に送信されてきたフレーム同期パターンの同期パターンの位置を決定する位置同期手段と、この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。



(2)

【特許請求の範囲】

【請求項1】 伝送路中に送信されてきたフレーム同期パターンが付加されている情報データを伝送する配線手段と、

この配線手段に伝送された情報データからこのフレーム同期パターンを抽出するフレーム同期パターン抽出手段と、

伝送路中に送信されてきたフレーム同期パターンの同期パターンの位置を決定する位置同期手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とするフレーム同期装置。

【発明の詳細な説明】

【0001】 図面上の利用分野 本発明は、図1に示されるフレーム同期装置に関する。

【0002】 従来の技術 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0003】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0004】 この方式では、フレーム同期装置と伝送路との間に、伝送路中に送信されてきたフレーム同期パターンを抽出するフレーム同期パターン抽出手段と、

伝送路中に送信されてきたフレーム同期パターンの同期パターンの位置を決定する位置同期手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。

【0005】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0006】 また、伝送路1から受信されるフレーム同期パターンと伝送路2から受信されるフレーム同期パターンとを比較して、伝送路2から受信されるフレーム同期パターンの位置を決定する位置同期手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。

【0007】 また、別のフレーム同期装置に、図1に示した方式である、この方式では、伝送路中に送信されてきたフレーム同期パターンを抽出するフレーム同期パターン抽出手段と、

伝送路中に送信されてきたフレーム同期パターンの同期パターンの位置を決定する位置同期手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。

【0008】 また、別のフレーム同期装置に、図1に示した方式である、この方式では、伝送路中に送信されてきたフレーム同期パターンを抽出するフレーム同期パターン抽出手段と、

伝送路中に送信されてきたフレーム同期パターンの同期パターンの位置を決定する位置同期手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。

【0009】 また、別のフレーム同期装置に、図1に示した方式である、この方式では、伝送路中に送信されてきたフレーム同期パターンを抽出するフレーム同期パターン抽出手段と、

伝送路中に送信されてきたフレーム同期パターンの同期パターンの位置を決定する位置同期手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。

【0010】 また、別のフレーム同期装置に、図1に示した方式である、この方式では、伝送路中に送信されてきたフレーム同期パターンを抽出するフレーム同期パターン抽出手段と、

伝送路中に送信されてきたフレーム同期パターンの同期パターンの位置を決定する位置同期手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。

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フレーム同期装置の配線手段は、同じにしておく必要がある。

【0008】 受信装置では、伝送路から送られてきたデータと、送信装置に入力されたフレーム同期パターンの位置を合わせてデータにフレーム同期パターンを付加する。

【0009】 また、データとフレーム同期パターンを付加する手段と、伝送路中に送信する手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。

【0010】 本発明は、従来のフレーム同期装置の構成とは異なり、伝送路中に送信されてきたフレーム同期パターンを抽出するフレーム同期パターン抽出手段と、

伝送路中に送信されてきたフレーム同期パターンの同期パターンの位置を決定する位置同期手段と、

この位置同期手段の検出結果に基づいて、配線手段から情報データを伝送する選択手段とを備えたことを特徴とする。

【0011】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0012】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0013】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0014】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0015】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0016】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0017】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0018】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0019】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0020】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0021】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0022】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

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【0024】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0025】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0026】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0027】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0028】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0029】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。

【0030】 図1は、ATMセルのような固定長のフレームを伝送するフレーム同期装置の構成を示す図である。





# PATENT ABSTRACTS OF JAPAN

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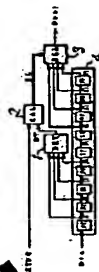
(21)Application number : 05-222928 (71)Applicant : TOSHIBA CORP  
(22)Date of filing : 08.09.1993 (72)Inventor : MOTOYAMA MASAHIKO

## (54) FRAME SYNCHRONIZING DEVICE

### (57)Abstract:

**PURPOSE:** To cope with the acceleration of a transmission speed and to eliminate the need of equalizing the lengths of wires and adjusting data phases by detecting frame synchronizing patterns from stored information data, obtaining a phase difference with transmitted frame synchronizing signals and synchronizing frames.

**CONSTITUTION:** A synchronizing pattern detection circuit 1 detects the frame synchronizing patterns from the information data stored in the shift register 4 of a storage means. The phase difference of the frame synchronizing pattern and transmitted synchronizing signals SYNC is calculated in a phase difference calculation circuit 2 and the head position of data inside the register 4 is decided by a selector 3. By this constitution, the need of equalizing the length of the wires and adjusting the data phase is eliminated and this frame synchronizing device capable of coping with the acceleration of the transmission speed is obtained.



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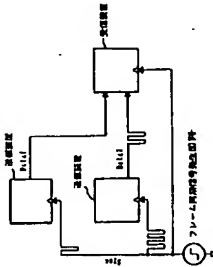
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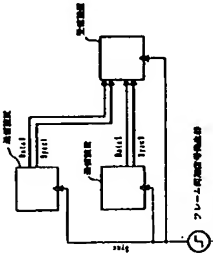
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(7)

(図12)



(図13)



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rejection]

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CLAIMS

[Claim(s)]

[Claim 1] A storage means to memorize the information data with which the frame synchronization pattern to which the inside of a transmission line has been transmitted is added, A frame synchronization pattern detection means to detect this frame synchronization pattern from the aforementioned information data memorized by this storage means, Frame synchronization equipment characterized by having a phase contrast operation means to search for the phase contrast of the frame synchronization signal and the aforementioned synchronous pattern which were inputted from the exterior, and a selection means to choose information data from the aforementioned storage means based on the result of an operation of this phase contrast operation means.

[Translation done.]

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## DETAILED DESCRIPTION

## [Detailed Description of the Invention]

[0001] [Field of the Invention] this invention relates to the frame synchronization equipment for taking the frame synchronization of the packet information to which the synchronous pattern information on a fixed length was given.

[0002] [Description of the Prior Art] Drawing 1.1 is drawing which expresses the frame synchronization method in the case of transmitting the frame of a fixed length [like] between equipments with ATM cell's. A sending set and a receiving set operate synchronizing with a common frame synchronization signal. Between a sending set and a receiving set, in order to take frame synchronization, you have to delay the frame synchronization signal inputted into a receiving circuit in consideration of the transit delay from a sending set to a receiving set.

[0003] Moreover, in order to make the same time delay between each sending set and a receiving set when the signal from two or more sending sets is inputted into a receiving set as shown in drawing, it is necessary to use an adjustable delay circuit.

[0004] In this method, in order to take frame synchronization, the amount of retardation needed to be adjusted, and there was a problem take time. Moreover, in consideration of the delay of the wire length on a substrate is beforehand calculated to another frame synchronization method, and the method which adjusts the wire length of the data signal line between equipments and a synchronizing signal is shown in drawing 1.2 is situated in it.

[0005] The phase with the frame synchronization signal inputted into the frame synchronization signal inputted into a sending set 1 and the sending set 2 is made the same, and the frame synchronization signal inputted into a receiving set is made to suit the phase which added the delay of the data from a sending set to a receiving set.

[0006] Moreover, it is necessary to make the delay of the data from a sending set 2 to a receiving set / the transmission line from a sending set 1 to a receiving set, J. In this method, there is a trouble where adjustment of a phase is difficult after assembling equipment, and the difficulty of merit-izing, such as a design pattern top, increases in connection with improvement in the speed of transmission speed.

[0007] Moreover, the method shown in drawing 1.3 is situated in another frame synchronization method. This method is a method to which data and a synchronizing signal are transmitted together. In this method, a sending set transmits a frame synchronization signal together with data. It is necessary to make the same the wire length of data and a frame synchronization signal.

[0008] In a receiving set, the data sent from the sending set are set by the phase of the frame synchronization signal into which it was inputted by the receiving set, and frame synchronization of data is performed. In this synchronous system, since a frame synchronization signal is transmitted together with data, there is a problem that the number of wirings increases. Moreover, there is also a problem that it must merit-ize [ wire length / of data and a frame synchronization signal ].

[0009] [Problem(s) to be Solved by the Invention] The conventional frame synchronization method had to be merit-ized [ wire length J, or had to adjust the phase of data, and had the trouble of the correspondence to improvement in the speed of transmission speed having become difficult, or taking the time of adjustment.

[0010] this invention was made in view of the conventional technical problem, and aims at offering the frame synchronization equipment into which it can correspond to improvement in the speed of transmission speed, and the time of adjustment of a wiring does not go.

[0011] [Means for Solving the Problem] In order to attain the above-mentioned purpose, it sets to this invention. A storage means to memorize the information data with which the frame synchronization pattern to which the inside of a transmission line has been transmitted is added. A frame synchronization pattern detection means to detect this frame synchronization pattern from the information data memorized by this storage means, it is characterized by having a phase contrast operation means to search for the phase contrast of the frame synchronization signal and synchronous pattern to which the inside of a transmission line has been transmitted, and a selection means to choose information

[http://www4.ipdl.jp/cg-bin/tran\\_web.cgi\\_ejje](http://www4.ipdl.jp/cg-bin/tran_web.cgi_ejje)

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data from a storage means based on the result of an operation of this phase contrast operation means.

[0012]

[Function] If this invention is used, a frame synchronization pattern detection means will detect a frame synchronization pattern from the information data memorized by the storage means, and it will be enabled to perform frame synchronization, without performing merit-izing, such as a wiring, and adjustment of a data phase by searching for the phase contrast with the frame synchronization signal transmitted in the inside of a transmission line.

[0013]

[Example] Hereafter, one example of this invention is explained using a drawing.

[Example 1] View 1 is drawing showing one example of this invention. This frame synchronization circuit consists of the shift register, a synchronous pattern detector (DET) 1, a phase contrast calculation circuit (CAL) 2 that calculates the phase contrast of a synchronizing signal and the synchronizing signal detected by the synchronous pattern detector (DET) 1, and a selection circuitry (SEL) 3 which chooses the head of a frame from the data in a shift register by the calculation result of the phase contrast calculation circuit (CAL) 2.

[0014] The data inputted into equipment are inputted into a shift register. It detects whether the synchronous pattern detector (DET) 1 has the same data stream as a synchronous pattern in the data memorized in the shift register 4.

When the same data stream as a synchronous pattern is in a shift register 4, it notifies that the synchronous pattern was detected to the phase contrast calculation circuit (CAL) 2.

[0015] In the phase contrast calculation circuit (CAL) 2, the phase contrast of the frame synchronization signal inputted apart from data and the frame obtained from the synchronous pattern detector (DET) 1 is calculated.

[0016] It notifies which data are chosen from the calculated phase contrast to a selection circuitry (SEL) 3. An operation of this equipment is explained using drawing 2.

[0017] This drawing is a timing chart at the time of using 4 bits for a synchronous pattern. A period should just use what is 4 for a synchronous pattern. For example, that from which 1 bit of a head and the remaining bit are different is shown in "1000", the thing from which data change in right in the middle as shown in "1100" can be used.

[0018] When an n-bit synchronous pattern is used, a period uses the data which is n. The synchronizing signal with which SYNC is inputted into equipment, and Din (0) A data input, then the phase of a synchronizing signal and data is in agreement, and Din (-1) A data input when the phase of a synchronizing signal is later than the phase of a synchronizing signal, and Din (+1) A data input when the phase of data is later than the phase of a synchronizing signal 1 bit, and DT, the output of the phase contrast calculation circuit (DET) 1 and SEL 3, and the output signal of the phase contrast calculation circuit (CAL) 2, and Dout. It is data output.

[0019] When there is no phase contrast of data and a synchronizing signal first, the case where it is Din (0) is explained. Din (0) is the case where the phase of a synchronizing signal and data is in agreement, and the output of the synchronous pattern detector (DET) 1 becomes like DT (0) at this time. The phase contrast calculation circuit (CAL) measures time after a synchronizing signal starts until the detecting signal of the synchronous pattern detector (DET) arrives. In this case, it is 5. Designation is taken out to a selection circuitry (SEL) 3 so that the output of the register with which the head of data is memorized based on the measured result may be chosen. In this case, the output of D8

[0020] Next, when the phase of data is later than the phase of a synchronizing signal 1 bit, the case of Din (-1) is explained. Din (-1) is in the case that the phase of data is quicker than the phase of a synchronizing signal 1 bit, and the output of the synchronous pattern detector (DET) 1 becomes like DT (-1) at this time. The phase contrast calculation circuit (CAL) 2 measures time after a synchronizing signal starts until the detecting signal of the synchronous pattern detector (DET) 1 arrives. In this case, it is 4. Designation is taken out to a selection circuitry (SEL) 3 so that the output of the register with which the head of data is memorized based on the measured result may be chosen. In this case, the output of D9 is chosen. The signal which directs selection is held until the head of the following frame comes.

[0021] Similarly, in Din (+1), the output of D7 is chosen, and when it is Din (+2), the output of D6 is chosen. The example of the phase contrast calculation circuit (CAL) 2 is shown in drawing 3. This phase contrast calculation circuit (CAL) 2 consists of a detector 5, and a counter 6 and two registers 8 and 9 in the standup of a synchronizing signal.

[0022] The circuit (EDGE) 5 which detects the standup of a synchronizing signal detects the standup of a synchronizing signal, and generates a pulse. A counter 6 is reset by the pulse signal which the standup detector 5 generates. A register (REG1) 8 loads the value of a counter 6 by the synchronous pattern detecting signal. This value becomes the phase contrast of data and a synchronizing signal. A register (REG2) 9 loads the value of a register (REG1) 8 by that to which the encoder 7 encoded the value which a counter 6 generates. That to which the encoder 1 encoded the value of this register (REG2) 9 is sent to a selection circuitry (SEL) 3. You may make reverse arrangement of a register (REG2) 9 and the encoder 10.

[0023] As mentioned above, if the phase simulation circuit of this invention is used and a n-bit synchronous pattern http://www4.ipdl.jp/cg-bin/tran\_web.cgi\_ejje

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will be given, it will be enabled to correct the phase gap to  $n$  bits automatically. Therefore, it is not necessary to form the length of a wiring into grade length correctly or, and becomes unnecessary to adjust phase contrast.

(Example 2) The configuration of the second example 17, two or more synchronous pattern detectors (DET) 11, 12, 13, and 14, a phase contrast calculation circuit (CAL) 15, and a selection circuitry (SEL) 16.

(00225) This drawing is showing the configuration at the time of using 4 bits to a synchronous pattern. Moreover, the synchronous circuit of this example can adjust phase contrast when 0-3 bits of data are behind the synchronizing signal.

(00226) The synchronous circuit of this example consists of the shift register of 8 bits, four synchronous pattern detectors (DET) 11, 12, 13, and 14, a phase contrast calculation circuit (CAL) 15, and a selection circuitry (SEL) 16. (00227) The configuration of the phase contrast calculation circuit (CAL) 15 of this equipment is shown in drawing 6. This phase contrast calculation circuit (CAL) 15 consists of a standup detector (DET) 18 of a synchronizing signal, a counter 19 reset in the standup of a synchronizing signal, and a register which memorizes the output of a synchronous pattern detector (DET).

(00228) The standup detector (DET) 18 detects the standup of a synchronizing signal, and generates a pulse. A counter is reset by the pulse generated by the standup signal. That is, it is reset in the standup of a synchronizing signal. A register memorizes the value of a synchronous pattern detector (DET) with the loading signal generated by the counter. The value memorized by the register shows the topology of data. The indication signal of a selection circuitry (SEL) is generable by encoding the value of a register. Reverse is sufficient as the arrangement sequence of an encoder and a register.

(00229) The operation at this time is explained using the timing chart of drawing 5. This timing chart shows the operation when the phase contrast of data and a synchronizing signal is in agreement.

(00300) The output of the phase contrast detector (DET) in this case serves as DT (= 0, DT 2 = 0, DT 3 = 0, and DT 4 = 1. Therefore, when there is no phase contrast of a synchronizing signal and data, the value of the register of a phase contrast calculation circuit (CAL) is set to "0001." In this case, the designation which chooses the signal of D8 is sent to a selection circuitry (SEL).

(00301) When data have sent 1 bit from the synchronizing signal, the value of the register of a phase contrast calculation circuit (CAL) is set to "0010." In this case, the designation which chooses the signal of D7 is sent to a selection circuitry (SEL).

(00302) When 2 bits of data are behind the synchronizing signal, the value of the register of a phase contrast calculation circuit (CAL) is set to "0100." In this case, the designation which chooses the signal of D6 is sent to a selection circuitry (SEL).

(00303) When 3 bits of data are behind the synchronizing signal, the value of the register of a phase contrast calculation circuit (CAL) is set to "1000." In this case, the designation which chooses the signal of D5 is sent to a selection circuitry (SEL).

(00304) Moreover, the configuration of a serial input parallel output which is shown in drawing 7 is also realizable. The synchronous circuit of this example consists of the shift register of 8 bits, four synchronous pattern detectors (DET), a phase contrast calculation circuit (CAL), and four selection circuitries (SEL). In this case, it is possible to share the shift register for synchronizing with a serial parallel converter. When the information developed parallel is required, compared with the case where a serial parallel converter is given to a synchronous circuit, a hardware scale can be made small by using such a configuration.

(035) As mentioned above, if a  $n$ -bit synchronous pattern is given, it will be enabled to correct the phase gap to  $n$  bits automatically. Therefore, the need of forming the length of a wiring into grade length correctly, or adjusting phase contrast becomes unnecessary.

(Example 3) The configuration of the third example is shown in drawing 8. In this drawing, the degree of parallel is set to 4 for the explanation. This example consists of a serial-parallel converter (SP), two or more shift registers (SR), a synchronous pattern detector (DET), a selection circuitry (SEL), and a phase contrast calculation circuit (CAL).

(0036) Drawing 10 is drawing showing the detailed configuration of the third example. The data inputted into this equipment are changed into a parallel data in a serial parallel transducer (SP). It is changed into a 4-bit parallel data in the example of drawing.

(0037) The data changed parallel are inputted into a shift register (SR), respectively. A shift register is prepared the same number of pieces as the degree of parallel. Four shift registers are prepared in this example.

(0038) Thus, in the data by which parallel expansion was carried out, if parallel expansion is carried out before taking frame synchronization, as shown in drawing 9, top data will become [ into which shift register it is inputted, and ] unfixed.

(0039) In order to detect the synchronous pattern over two or more shift registers, it is necessary to use a synchronous pattern detector which is shown in drawing 11. This synchronous pattern detector detects a synchronous pattern ranging over two or more shift registers. DET1 detects the synchronous pattern at the time of being inputted in the

order of SR1, SR2, SR3, and SR4, namely, DET2 The synchronous pattern at the time of being inputted in the order of SR2, SR3, SR4, and SR1 is detected. DET3 The synchronous pattern at the time of being inputted in the order of SR3, SR4, SR1, and SR2 is detected, and DET4 detects the synchronous pattern at the time of being inputted in the order of SR4, SR1, SR2, and SR3. In this example, it is a detector in case a synchronous pattern is "1000."

(0040) The synchronous pattern detected by the detector is sent to a phase contrast calculation circuit. In a phase contrast calculation circuit, with an encoder, coding of the inputted synchronous pattern is carried out, and it is memorized by the register. The timing loaded to a register is generated on the basis of the standup information on the frame synchronization signal. Therefore, the information memorized by the register includes the information on the phase of data, and the phase contrast of a frame synchronization signal.

(0041) The value of this register is sent to a selection circuitry (SEL). A selection circuitry (SEL) as well as a synchronous pattern detector (DET) chooses data ranging over two or more shift registers. Thus, by things, after developing data parallel, it is enabled to take frame synchronization.

(Effect of the Invention) If this invention is used as explained in full detail above, a phase contrast operation means will be based on the ability of phase contrast to be searched for using the frame synchronization pattern and frame synchronization signal which were detected by the frame synchronization pattern detection means, and since the selection output is carried out of the information data with which the selection means is memorized by the storage means, it will be enabled to perform frame synchronization without needing adjustment of the amount of retardation etc. by small-scale hardware.

[Translation done.]